AMENDMENTS TO THE CLAIMS

1.(original): A synchronization tracking circuit for synchronizing the phase of a despreading code sequence on a receiving side to the phase of a spreading code sequence on a transmitting side, comprising:

a DLL circuit for performing synchronization tracking by DLL (Delay Locked Loop) control; and

an interference-component estimation unit for estimating an interference component inflicted by another path upon a prescribed path of interest among multiple paths;

wherein said DLL circuit executes DLL control for causing the phase of the despreading code sequence on the receiving side to be synchronized with and track the phase of the spreading code on the transmitting side based upon a signal obtained by eliminating the interference component, which is inflicted from the other path, from a despread signal obtained by despreading a receive signal.

2.(currently amended): The circuit according to claim 1, wherein said interference-component estimation unit estimates the interference component inflicted by the other path upon

a phase control signal generator for generating a signal for controlling the phase of the despreading code sequence on the receiving side based upon the despread signal from which the interference component has been eliminated.

4.(original) The circuit according to claim 1, wherein said DLL circuit eliminates only an interference component from another path for which a path-to-path delay-time difference between this other path and the path of interest is less than a threshold value.

5.(original) The circuit according to claim 2, further comprising an impulse response generator for storing impulse response values discretely and outputting an impulse response value that corresponds to an interpath delay-time difference;

wherein said impulse response generator approximates an impulse response value by $1/2^n$ of a peak value (where n is a positive integer) and includes:

a storage unit for storing correspondence between time and n discretely; and

an arithmetic unit for obtaining n of a time that conforms to the interpath delay-time difference and calculating an impulse response value upon shifting the peak value by n bits.

6.(original) The circuit according to claim 3, wherein said despreader generates first and second despread signals by despreading the receive signal at a timing that leads, by a predetermined phase, timing of the spreading code sequence on the transmitting side and at a timing that lags, by a predetermined phase, timing of said spreading code sequence;

said interference-component elimination unit eliminates an interference component from each despread signal; and

said phase control signal generator obtains the power of each despread signal from which the interference component has been eliminated and generates a signal for controlling the phase of the despreading code sequence on the receiving side based upon a

difference betwee the powers obtained.

7.(original) The circuit according to claim 3, wherein said despreader generates first and second despre d signals by despreading the receive signal at a timing that leads, by a predetermined pha e, timing of the spreading code sequence on the transmitting side and at a timing that lags, b a predetermined phase, timing of said spreading code sequence;

sai interference-component elimination unit eliminates an interference component from e ch despread signal; and

sai phase control signal generator rotates, on the basis of a channel estimation value of the path o interest, phase of a difference signal between despread signals from which an interference comp nent has been eliminated, and generates a signal for controlling the phase of the despreading c de sequence on the receiving side based upon a signal obtained by the phase rotation.